PhD Thesis Proposal Form
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FIELD open

Thesis subject title: Energy-Quality-Time Fault Tolerant Task Mapping on Multicore Architectures

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- Thesis proposal (max 1500 words):

The safety-critical domain industries usually consist of mixed-critical systems [7], where guarantees must be provided on safety and reliability for the high-criticality applications, implying both high **fault tolerance** and hard **real-time** constraints. For example, avionics systems consist of applications with different Design Assurance Levels (DAL) [1] operating in high altitudes exposed to radiation. Space systems consist of navigation control applications and scientific applications operating in outer space with extreme particle and high-energy electromagnetic radiation. Automotive systems have applications in the same wheel sensor for stability control and for the acceleration regulation while they suffer from alpha particles, high temperature peaks and electromagnetic interferences [8]. These natural and technical stimuli are the source of faults that impact the system functionality [4]. Within last thirty years, the code size of automotive, space and avionics applications has significantly increased [9]. The mixed-critical systems face exponential growth in performance requirements, whereas future automotive and aerospace applications will require higher performance computing resources [7].

At the same time, the consumer market has shifted towards **multicore** architectures, due to power consumption and heat dissipation limits of single processors [7]. Multicores provide a Space, Weight and Power reductions (SWaP) and massive computing capabilities compared with single core processors, while they can integrate diverse applications on the same platform [3]. As the consumer market redefines the way of designing future embedded and complex systems, there is a clear need to integrate both high-criticality and low-criticality functionalities on a multicore [7]. However, no established approach exists yet to achieve the safety certification on multicore architectures [2], especially due to two main scientific challenges raised by the use of multicores.

The first challenge is the sharing of resources among cores, e.g. the interconnection network on chip, the

memories and controllers. Integrating high-criticality and low-criticality applications on the same multicore leads to potential concurrent accesses to the shared resources highly affecting the applications timing behaviour, which is of paramount importance for the high-criticality applications. To provide a deterministic timing behaviour, either Worst Case Execution Time (WCET) bounds are computed or spatial and temporal isolation is applied. In both cases, the result is a sub-optimal use of the available resources. During WCET estimations, the worst case has to be considered: at every access to a shared resource by a core, it is assumed that the remaining cores are accessing the same resource at the same time. As result, the WCET estimations considering the complete application are pessimistic and, thus, lead to over-provisioning the resources to the high-criticality applications. On the other hand, the isolation prohibits the use of the resources by the low-criticality applications, whenever the high-criticality applications do not need them any more. To improve the global system Quality-of-Service (QoS), while guaranteeing the hard real-time deadlines, the applications have to be further analysed to identify the parts that are mandatory to be executed and have high safety requirements.

The second challenge is that the multicore platform itself is susceptible to faults due to the nature of electronic systems. Combined with the reduction of the transistors size and the technology, the multicores are becoming more and more sensible to the operating conditions and to the environmental impact [5]. In electronic systems, the variation on the threshold voltage depends on the transistor width, whereas voids or small cracks in the wiring lead to close or open source problems. The current or voltage activity and the hot spots are inevitable during the system operation, but they cause electromigration, Bias Temperature Instability and crosstalk, which are sources of faults. To improve the multicore reliability, either radiation-hardened processors are used or the architecture is replicated [6]. The former solution develops systems with limited computation capabilities and it requires a difficult-to-find design expertise, which combines digital and analogue electronics with semiconductor physics. The latter solution has high cost and energy consumption. To reduce the cost, while providing reliability, the resources replication and the system oversizing has to be avoided, whenever possible.

In addition, the **energy consumption** has become an important concern, especially for systems with limited energy budget, such as battery powered or energy-harvesting Internet of Things (IoT) devices. Smartphones use a heterogeneous multicore architecture called big.LITTLE, which consists of performance-optimized big cores and energy-optimized little cores with a single ISA (Instruction Set Architecture) [10]. Recently released embedded boards for IoT such as Raspberry Pi, Odroid, Edison, Jetson, and Artik also provide multiple cores [11–13]. The use of multiple cores supports efficiently the IoT services, but it inserts a new challenge. The increase in the number of cores puts pressure on the energy resource of the device since the power and energy consumptions are increased [14]. Hence, multicore platforms have been enhanced with the capability of scaling their voltage and frequency during execution to balance system performance and energy saving. In order to fully exploit the features of multicore systems, while meeting system specifications, mechanisms are required to decide the efficient execution of the tasks on such multicores with scalable operating features.

The goal of this thesis is to address the combined challenge of mixed-criticality and fault tolerance on multicores. On the one hand, several applications in mixed critical systems accept approximate results as long as the baseline Quality of Service (QoS) is satisfied [19]. For instance, frames of fuzzy images in image processing applications and rough estimates of location in tracking applications produced in time are better results than perfect images and accurate location produced too late. In these domains, the applications can be modelled as Imprecise Computation (IC) tasks, where a task is logically decomposed into a set of mandatory subtask and a set of optional subtasks. The mandatory subtasks must be completed before the deadline to have an acceptable result, while the optional subtask can be left incomplete at the cost of reduced quality. The QoS of the intermediate results is increased as the optional subtask is executed longer. On the other hand, Dynamic Voltage Frequency Scaling (DVFS) is a technique to manage both voltage and frequency for controlling the consumed energy of the system. In this thesis we are interested in combining DVFS and IC tasks to decide the

execution of the tasks on multicore architectures in order to maximize QoS and reliability, while satisfying the real-time and the energy constraints.

The way the IC tasks are executed on a platform is decided by several factors. The first factor is the task mapping, which refers to both the task allocation (on which core each task is executed) and the task scheduling (when each task starts execution). The second factor is the decision of the voltage and frequency of the core when it runs a specific task. The third factor is the determination of how long the optional part of each task, whereas the fourth factor is the decision over the level of redundancy. Existing works that focus on the pure *energy-aware task mapping problem* aim at minimizing energy consumption under resource and timing constraints. Usually they are based on DVFS techniques [15-16], whereas the task model does not consider imprecise computation. As the tasks are not modifiable, thus, no exploration of the QoS through the optional subtasks is considered. Other approaches solve the *QoS-aware task mapping problem* using the IC task model and having as goal to maximize QoS under energy supply and real-time constraints. However, they focus on single core [17] or multicore platforms without DVFS capabilities. The existing approaches on multicores consider that the task allocation is upfront given or they carry out task allocation and adjustment separately. The complex coupling between the optimization variables of these problem formulations prohibits the algorithms to achieve the optimal solution. Therefore, they propose sub-optimal methods based on 1) problem approximation/relaxation, and 2) heuristics. The QoS-aware task mapping is still an open issue, since there is no optimal polynomial-time solution [18]. Compared with the existing approaches, the thesis focuses on designing novel methodologies to efficiently solve the problem of task execution on multicore platforms by jointly addressing all four aforementioned factors. We are interested in both optimal solution found with reduced computation time and approaches able to degrade the obtained solution in a controlled way.

The benefits of this thesis are the integration of mixed-critical applications on a multicore platform meeting real-time, energy and reliability requirements, while supporting the replacement of the existing infrastructures leading to a significant reduction of the physical system components, and, thus, it reduces the system cost, energy and maintenance, while it highly increases reliability [12].

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- Publications of the laboratory in the field (max 5):

[1] L. Mo, A. Kritikakou and O. Sentieys, "Decomposed Task Mapping to Maximize QoS in Energy-Constrained Real-Time Multicores," *2017 IEEE International Conference on Computer Design (ICCD)*, Boston, MA, 2017, pp. 493-500.

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- Joint Phd (cotutelle) :   NO
- Co-directed PhD :   YES

In case of a co-directed or a joint PhD, please detail:

- Partner university name: University of Rennes 1

- Laboratory name and web site: IRISA, https://team.inria.fr/cairn/

- PhD co-director (contact person):

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- Provisional duration and timetable of the PhD student's stay at ENS Rennes:
  The duration of the PhD is expected to be at maximum 4 years.

- If previous collaborations with the Chinese co-director/university, please detail:
  The University of Rennes 1, where both the PhD director and the co-director belong to, had a common Master program (M2 Embedded System) with the Southeast University in Nanjing, China. Several members of our team, CAIRN, have travelled to China and given courses under this collaboration. In addition, we have active research collaboration through our postdoctoral researcher Lei Mo with the following universities: Zhejiang University, Hangzhou (Prof. Jiming Chen) in collaborative estimation and control on Wireless Sensor and Actuator Networks, South China University of Technology, Guangzhou (Prof. Bugong Xu) on distributed control in Wireless Sensor Networks, and the Southeast University, Nanjing (Prof. Xianghui Cao) on resource optimization on Cyber-Physical Systems. The PhD director also has active collaboration in combinatorial optimization problems for custom processors with his former PhD student, Chenglong Xiao, who is currently an associate professor in the school of software engineering at the Liaoning Technical University.

- Interest of the Joint PhD for the French co-director, for his/her laboratory, for ENS Rennes:
  Our motivation for the PhD is to establish a long-term collaboration also in research with a team in China in the domain of embedded systems and especially multicore-manycore architectures. We strongly believe that this PhD will promote international exchanges and cooperation, as it allows our team to recruit students with high technical skills required in our domain and at the same time opens opportunities for potential collaboration in international research projects with Chinese universities, research centers and innovation companies.

Date: 15/01/2018

Signature of the PhD director   Name and signature of the Laboratory director
                                                 Jean-Marc JEZEQUEL