PhD Thesis Proposal Form
China Scholarship Council (CSC)/ENS Rennes
Call for projects 2022

FIELD: Computer science

THESIS SUBJECT TITLE: Efficient High-level Synthesis Design Space Exploration Based on Cloud Computing

1. Single French PhD proposal:

- Laboratory name: IRISA (http://www.irisa.fr/en)
  CAIRN team (https://team.inria.fr/cairn/)
- PhD director (contact person):
  - Name: Emmanuel Casseau
  - Position: Professor
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  - Phone number: + 33 2 96 46 91 76

2. Co-directed or a joint PhD, please specify:

- Joint PhD (cotutelle): ~~YES~~ or **NO**
- Co-directed PhD: **YES** or ~~NO~~

- Partner university name: Shantou University, China
- Laboratory name and web site: College of Engineering (https://eng.stu.edu.cn/)
-
- PhD director-s in partner university (contact person):
  - Name: Chenglong Xiao
  - Position: Professor
  - E-mail: chlxiao@stu.edu.cn
  - Phone number: +86-15142813892

- If previous collaborations with the Chinese co-director/university, please detail:

  We have active research collaboration with Prof. Chenglong Xiao, who is the co-director of this proposal and who was previously a PhD student in our IRISA lab and now is with the Shantou University of China. We have 10 common publications related to the subject of this thesis proposal, with 5 articles published in renowned internationals journals (IEEE TCAS II, Journal of Systems Architectures, Microprocessors & Microsystems and Integration, the VLSI journal), and 5 articles published in well-known conferences (ISCAS, GLSVLSI, ASAP, DASIP).

  We have also active joint collaboration in research projects: the co-director and PhD director were, respectively, the Principal Investigator and the main participant of a research project funded by National Natural Science of China (Automatic Custom Instruction Identification for Improving High-level Synthesis Effectiveness, No. 61404069).

  Furthermore, the University of Rennes 1, where the PhD director belongs to, has established long-term collaboration with Universities in China (e.g., a common Master program (M2 Embedded System) with the Southeast University in Nanjing). Several members of our team, CAIRN, have travelled to China and have given courses under this collaboration.

- Interest of the Joint PhD for the French co-director, for his/her laboratory, for ENS Rennes:

  Our motivation for the PhD is to further establish a long-term research collaboration with Chinese Universities, especially with the Shantou University of China, in the domain of electronic design automation (EDA) and especially high-level synthesis. We strongly believe that this PhD will promote international exchanges and cooperation, as it allows our team to recruit students with high technical skills required in our domain and at the same time opens opportunities for potential collaboration in international research projects and student exchanges with Chinese universities, research groups and innovation companies.

- Thesis proposal (max 1500 words):

  Key words : High-level synthesis, design space exploration, cloud computing, machine learning

  The rapid development of integrated circuit technology and the increasing complexity of applications force the development of integrated circuit design methods and tools to a higher level of abstraction. Actually the hardware design at the traditional register transfer level (RTL) is very cumbersome, time-consuming and error prone. Because the design at RTL level involves a huge amount of code (for example, about 7 million lines of RTL code are required for the design of 50 million gates of integrated circuits), changing a micro-architecture requires modifying many files and modules, sometimes taking several weeks to modify relevant files and modules.

  In order to better deal with the multiple challenges of emerging markets such as artificial intelligence, 5G, automatic driving, high-level design is a bridge connecting the future. **High-level synthesis** (HLS) is a process of automatically transforming high-level behaviour descriptions (such as C, C++ or SystemC) into circuit models described in low-level language. Using high-level description for design, the corresponding amount of code is reduced by about 10 times compared with RTL level hardware description code. Therefore, using HLS can significantly shorten the design time and reduce the cost.

  HLS can generate several functional equivalent candidate design solutions without modifying the behaviour level description. This allows designers to conduct **design space exploration** (DSE) on the hardware design solution, so as to select the micro-architecture that can better meet the requirements of the project. DSE is one of the most crucial steps involved in high-level synthesis because the total number of synthesis options combinations is extremely large. Previous studies have shown that the design space exploration problem is a multi-objective optimization problem with exponential complexity. In practice, for complex applications, the existing methods may not be able to produce high-quality design solutions in a reasonable time.

  As the semiconductor technology moves towards 5-nm technology and below, the scale and complexity of chip design increase year by year, requiring higher computing performance and larger storage space. Deploying electronic design automation **(EDA) tools in the cloud** can provide flexible computing and storage resources according to the actual requirements of users, significantly reduce design time and cost, accelerate product launch time, etc. Thus cloud EDA is becoming more and more the trend of electronic design automation. For example, a typical 7-nm design rule checking (DRC) file may have up to 10000 complex rules. It takes about 100000 DRC calculation operations to implement these rules. The non-cloud detection of 7-nm full-chip DRC may take several days to complete an iteration. Using the IC validator deployed in cloud by Synopsys can shorten the iteration time to several hours.

  Back to HLS and DSE, the estimation of the quality of result (QoR) of each design plays a key role because the real quality of the resulting hardware designs is hard to predict. Previous methods are

mainly based on the quality results generated by the high-level synthesis tools: either directly call the HLS tools to give QoR, or simulate the high-level synthesis evaluation process to give QoR, or take the evaluation results given by the HLS tools as samples to train the prediction model to produce QoR. However, previous work also revealed that using a commercial high-level synthesis tool for FPGA design may produce 125% relative error with the final implementation when estimating the number of hardware resources. Thus, a more accurate QoR prediction model is required.

Considering the exponential complexity of the design space, most of the existing studies use meta-heuristic methods and specific exploratory methods to provide only the approximate Pareto-optimal designs. In order to speedup the search of Pareto-optimal designs, a multi-threaded parallel search method can be used. However, it is still only suitable for simple applications or components. To cope with this issue, cloud computing based approaches seems very promising.

The aim of this thesis is to propose a **cloud computing based high-level synthesis design space exploration framework**. The detailed objectives include:
（1）a QoR prediction model with high accuracy: the accuracy of the QoR prediction model has an important impact on the subsequent design stages of high-level synthesis, and will determine the quality of the final integrated circuit.
（2） an efficient parallel design space exploration method based on cloud computing: design space exploration has exponential complexity and is a typical computing intensive task. Using cloud computing to explore design space can significantly accelerate the search process, and provide a set of Pareto optimal design solutions.

The specific research contents include:

(1) modelling the design space exploration problem as a **multi-objective optimization problem**, including latency, area and power consumption;
(2) using **machine learning methods** to quickly and accurately evaluate the delay, area and power consumption of candidate design solutions: we will first compare different supervised machine learning methods and choose some machine learning algorithms (e.g., GNN, RNN) as candidate methods. Then, we will study the relationship between features and QoR in training samples and the impact of supervision signal on prediction results, so as to extract features, reduce data dimension (delete redundant features and irrelevant features) and select supervision signals. Finally, we will design the parallel training approaches, and compare their influence on the accuracy of the results through experiments;
(3) studying how to reasonably divide the design space exploration problem into subproblems and **automatically allocate them to the cloud** for efficient parallel searching. Goal is to ensure load balance between computing nodes.

The benefits of this thesis is to establish a cloud-based design space exploration framework, in order to greatly shorten the design time of high-level synthesis and generate more accurate integrated circuit design solutions with higher quality despite a high-level abstraction based design approach such as HLS.

- Publications of the laboratory in the field (max 5):

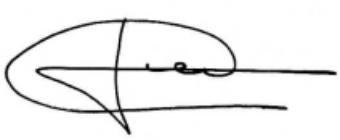
[1] C. Xiao, S. Wang, W. Liu, X. Wang, E. Casseau, An Optimal Algorithm for Enumerating Connected Convex Subgraphs in Acyclic Diagraphs, IEEE Transactions on Circuits and Systems II: Express Briefs, 68(1): 261-265, 2021.

[2] C. Xiao, S. Wang, W. Liu, E. Casseau, Parallel Custom Instruction Identification for Extensible Processors, Journal of Systems Architecture, 76:149-159, 2017.

[3] C. Xiao, E. Casseau, S. Wang, W. Liu, Automatic Custom Instruction Identification for Application-specific Instruction Set Processor, Microprocessors and Microsystems, 38(8):1012-1024, 2014.

Date: November 25, 2021

Signature of the PhD director
Emmanuel CASSEAU



Name and signature of the Laboratory Director
Guillaume GRAVIER